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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary**Application No.**

09/918,380

Applicant(s)

LAKSONO ET AL.

Examiner

Nhon T. Diep

Art Unit

2621

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 November 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 13, 15-29, 31-40, 43-50 and 52-57 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 13, 15-29, 31-40, 43-50 and 52-57 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 7/30/2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 11/06/2008 have been fully considered but they are not persuasive.

Regarding to the applicants' argument that "Eifrig does not disclose or render obvious that the scheduler 350 (alleged as the claimed DIP sequencer) configures a processor based on one or more packets obtained from a memory as provided by claims 13, 44, and 53. Rather, these passages merely teach that processing of pictures is controlled by the scheduler 350. Controlling the processing of pictures is not the same as, or even equivalent to, configuring a processor based on one or more packets as provided by the claims, and the Office has not provided any evidence or rationale to the contrary. In fact, other than citing the above- identified passages of Eifrig, no explanation of how Eifrig teaches a DIP scheduler to configure a processor based on one or more packets accessed from memory by the DIP scheduler. Thus, the Office fails to establish a prima facie case of obviousness for at least this reasons.". The examiner respectfully disagrees.

In addition to figure 3b, figure 4 illustrates the manipulation of picture queues using schedulers, and that figure 4, el. 402, 408, 412, 409, 414, 320 and col. 15, ln. 19 - col. 17, ln. 60, shows a high-level description of the Demux process 306 is given below. The Demux process examines all incoming MPEG transport stream (MTS) packets from the TCI 308. All packets that are not part of the audio or video PID streams for one of the services being transcoded on this TPE are removed. Audio transcoding is not

discussed here. The audio stream retains the same MTS and PES packet structure and will be output as part of the same service after the transcoding system delay. The transmux is a constant delay device and the same delay applies to all components of all services on all TPEs.. The Demux 306 decomposes the transport stream and de-packetizes elementary stream syntax for the video components and identifies the individual video access units (i.e., coded pictures). A video access unit consists of the coded picture plus all higher level syntax preceding the picture, and any stuffing bytes following the last slice of the picture. Once the access unit has been identified, a picture structure is allocated. Selected MTS and PES layer information to be preserved is stored in the picture structure (for inclusion in the output PES and MTS syntax). The Demux process 306 scans the video elementary stream for startcodes to identify the access units (coded pictures). It must also determine the size (in bytes) of the coded picture and the presentation duration of each picture (from the coded frame rate and the repeat_first_field flag). The picture size is used to determine when a complete picture is available in the input rate buffer (iRB), and is also used to calculate needed parameters for the statmux and rate-control. The presentation duration is used to construct a DTS for this picture in the event that it is not present in the PES packet. The current offset between the local 27 MHz clock and the program clock at the beginning of this picture is determined and stored in the picture structure; further more, scheduler 2 waits to get the DTS needed to decode picture and re-encode the pictures again. It is the examiner's opinion that Eifrig indeed discloses the limitation as argued.

Regarding to the applicants' argument that "Eifrig fails to disclose or render obvious the above-identified claim features. The Office relies on Pian merely to support a theory that implementing the features of the claims in two separate processors as provided by the claims would be obvious. Office Action, pp. 6-7. The Office does not assert that Pian discloses the above-identified claim features, nor does Pian in fact disclose or render obvious these claim features.

Moreover, independent claims 13, 44, and 53 recite subject matter directed to a first processor and a second processor and their respective functionality/operations. For each of claims 13, 44, and 53, the Office asserts that element 10 ("parsing/demux 10") of FIG. 1 of Eifrig represents the claimed "first processor" feature and that element 30 ("core transcoding 30") of FIG. 1 of Eifrig represents the claimed "second processor" feature. See Office Action, pp. 2, 4, and 6. As discussed in greater detail at pages 9-12 of the Response filed May 7, 2007 (hereinafter, "the First Response") and at pages 9-11 of the Response filed November 20, 2007 (hereinafter, "the Second Response"), and as acknowledged by the Office at page 6 of the Office Action, Eifrig fails to disclose that element 10 and element 30 are implemented as separate processors. In fact, Eifrig expressly teaches that element 10 and element 30 are implemented at the same Very Long Instruction Word (VLIW) core. See, e.g., Eifrig, col. 4, lines 6-33 ("a) MPEG transport stream decoding (on VLIW core)(10)[...] c) Core transcoding (on VLIW core)(30)[...]") (emphasis added). As also discussed in the First Response and the Second Response, one of ordinary skill in the art will recognize that the parsing/demux

(element 10) and the corresponding core transcoder (element 30) conventionally are implemented together as a single processor.

The Office responds to the failure of Eifrig to contemplate separate processors by turning to Pian, which the Office alleges as teaching "in figure 1, elements 10 and 12, that a preprocessor and an encoder can be constructed as two separate processors. And, therefore, it would have been obvious... to modify the system of Eifrig et al by' constructing a preprocessor and [a] transcoder as two separate processors as taught by Pian et al as a matter of various variance [sic] *..". Office Action, p. 7. Contrary to the Office's assertions, nowhere does Pian disclose or suggest that the preprocessor 10 and the encoder 12 are constructed as separate processors. For example, while the preprocessor 10 and the encoder 12 as represented in FIG. 1 of Pian using different boxes, nowhere does Pian attribute any particular meaning to this use of different boxes as being associated with separate processors, and one of ordinary skill in the art would correctly interpret the use of different boxes for the preprocessor 10 and the encoder 12 merely as a common format for partitioning the different functions provided by each. Further, at the passage at col. 4, lines 38-42, Pian teaches that the "encoder 12 and rate controller 14[] are implemented in a microprocessor or digital signal processor programmed to provide the functions as described" but fails to disclose or even suggest that the preprocessor 10 is implemented in a second processor separate from the "microprocessor or digital signal processor" in which the encoder 12 is implemented. Thus, as neither Eifrig nor Pian discloses or suggests separate processors, the

combination of Eifrig and Pain fails to disclose or suggest separate processors.". The examiner respectfully disagrees.

First, one notes that the pre-processor is indeed separate from the compressor, because it can be bypassed completely (i.e. "excluded") from the normal operation of the disclosed encoder (Pian: column 4, lines 1- 4). Therefore, since it is not integral to the operation of the encoder, it is clearly separate. Now, we come to the whether the both the pre-processor and the encoder are both processing entities. The Examiner notes that by inherency, the label "preprocessor" explicitly encompasses a processing function. Additionally, we turn to Pian to characterize the processing capabilities of the compression system. In particular, the reference clearly notes that the preprocessor provides or formats the signal for easier processing by the compression system (Pian: column 4, lines 4-10). Therefore, the Examiner maintains that when analyzed as such, Pian clearly discloses the use of "separate processors" in a manner that would make obvious the incorporation of the doctrine of separation that has been staunchly established as unpatentable by the Courts, Nerwin v. Erlichman, 168 USPQ 177, 179, (PTO Bd. of Int. 1969).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 13, 15-29, 31-40, 43-50, 52-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eifrig et al (art of record), in view of Pian et al (US 6,366,614).

Eifrig et al discloses a transcoder-multiplexer architecture comprising the same integrated single chip system comprising: a memory (fig. 3a, el. 306 and buffer 310); a memory controller to access the memory (fig. 3b, el. 350); first processor to parse received video data to generate a plurality of packets and provide the plurality of packets for storage in the memory, the first processor comprising a general purpose processor (fig. 1a, el. 10 and col. 3, ln. 17-19 and also fig. 3a, el. 306 and buffer 310); a second processor comprising a video transcoder (fig. 1a, el. 30); and a decoder instruction packet (DIP) sequencer to access one or more packets of the plurality of packets from the one or more packets; and provide the one or more packets to the second processor for transcoding (fig. 3b, el. 50 and col. 8, lines 6-14, 34-36) as specified in claim 13; wherein the second element further includes: a data decompression portion; a scalar; and a data compression portion (col. 4, ln. 11-25) as specified in claim 15; wherein the decompression portion includes a portion to perform a frequency domain to time domain transform (IDCT) as specified in claim 16; wherein the frequency domain to time domain transform portion is a portion to perform an inverse discrete cosine transform portion as specified in claim 17; wherein the decompression portion includes a portion to perform a de-quantization of data (IQ) as specified in claim 18; wherein the decompression portion includes a portion to perform a DeZigZag of data (VLD) as specified in claim 19; wherein the decompression portion includes a motion compensation portion (fig. 6, el. 620) as specified in claim 20; wherein the

decompression portion includes a motion compensation portion (fig. 6, el. 620) as specified in claim 21; wherein the decompression portion includes a motion compensation portion (fig. 6, el. 620) as specified in claim 22; wherein the compression portion includes a motion vector generator (MV as inputted to el. 620) as specified in claim 23; wherein the motion vector generator includes a buffered motion predictor (el. 630, 640) as specified in claim 24; wherein the compression portion further includes a portion to perform a time domain to frequency domain transform (col. 4, ln. 17) as specified in claim 25; wherein the time domain to frequency domain transform portion includes a discrete cosine transform portion (col. 4, ln. 17) as specified in claim 26; wherein the compression portion includes a motion vector generator (MV as inputted to el. 620) as specified in claim 27; wherein the motion vector generator includes a buffered motion predictor (el. 630, 640) as specified in claim 28; wherein the second processor is coupled to the first processor through a memory controller and a sequencer (col. 6, ln. 6-41) as specified in claim 29; a method comprising: receiving, at a first element, a data stream including video data; parsing, at the first processor, the data stream to identify video data associated with a first channel (fig. 1a, el. 10 and col. 3, ln. 17-19 and also fig. 3a, el. 306 and buffer 310); packetizing, at the first processor, the video data associated with the first channel to generate the one or more packets, each packet having a video data payload and information related to the video data payload, wherein the video data payloads of the one or more packets represent a first channel of compressed video data having a characteristic represented by a first value (output to el. 20); storing the one or more packets at a memory (fig. 3a, el. 306 and

buffer 310); accessing, the one or more packets from the memory second processor, the one or more packets from the memory via a decoder instruction packet (DIP) sequencer; providing, from the DIP sequencer, the one or more packets to a second processor; configuring, via the DIP sequencer, the second processor based on opcodes of the one or more packets (fig. 3b, el. 350 and col. 8, ln 6-14 and 34-36); and transcoding, at the second processor, the video data payloads of the one or more packets to generate a representation of a second channel of compressed video data having the characteristic represented by a second value (fig. 1a, el. 30) as specified in claims 44 and 53; wherein the characteristic is a compression factor (fig. 6, el. 650) as specified in claims 31-32 and 45-46; wherein transcoding the video data payloads comprises: decompressing the video data payloads to generate a first intermediate data; scaling the first intermediate data to generate a second intermediate data; and compressing the second intermediate data to generate the representation of the second channel (fig. 1a, el. 30 and fig. 6) as specified in claim 33; wherein transcoding the video data payloads comprises: decompressing the video data payloads to generate a first intermediate data, wherein the first intermediate data is frequency domain data; converting the first intermediate data to a second intermediate data, wherein the second intermediate data is time domain data having the characteristic represented by the first value; converting the second intermediate data to a third intermediate data having the characteristic represented by the second value; and compressing the third intermediate data to generate the representation of the second channel (figs. 6, 7, 8) as specified in claim 34; wherein receiving the one or more packets includes: storing the video data

payloads of the one or more packets in a first memory of the second element; and storing the information associated with the video data payloads in a second memory of the second element (fig. 6, el. 630, 640) as specified in claim 35; wherein the video data payloads are transcoded based at least in part on the information associated with the video data payloads (MV-620-615-A1-Q2) as specified in claim 37; wherein the information associated with a video data payload indicates that the video data payload includes one or more of video time stamp information, picture configuration information, slice information, macroblock information, motion vector information, quantizer matrix information, or specific picture location information (MV) as specified in claim 38; wherein receiving the one or more packets and transcoding the video data payloads support a real-time play back of the representation of the second channel (col. 23, ln. 64 – col. 24, ln. 7) as specified in claim 39; further comprising: providing the representation of the second channel of compressed video data for reception by at least one multimedia device (fig. 1a, output of el. 40) as specified in claim 40; wherein the first data element includes a general purpose element and the second data element includes a video element (el. 10, 30) as specified in claim 43; wherein the first data processor is further to: decompress the video data payloads to generate a first intermediate data (fig. 1a, el. 20); scale the first intermediate data to generate a second intermediate data (fig. 6, el. Q2); and compress the second intermediate data to generate the representation of the second channel (fig. 6, el. 680) as specified in claim 47; wherein the first processor is further to: decompress the video data payloads to generate a first intermediate data, wherein the first intermediate data is frequency

domain data; convert the first intermediate data to a second intermediate data, wherein the second intermediate data is time domain data having the characteristic represented by the first value; convert the second intermediate data to a third intermediate data having the characteristic represented by the second value; and compress the third intermediate data to generate the representation of the second channel (fig. 6, DCT, IDCT, Q1, Q2) as specified in claim 48; wherein the first processor transcodes the video data payloads based at least in part on the information associated with the video data payloads (MV) as specified in claim 49; wherein the information associated with a video data payload indicates that the video data payload includes one or more of video time stamp information, picture configuration information, slice information, macroblock information, motion vector information, quantizer matrix information, or specific picture location information (MV) as specified in claim 50; wherein the first data element comprises a video element and the second data element comprises a general purpose element (fig. 1a, el. 10, 30) as specified in claim 52; and Parsing/Demux 10 and Code transcoding 30 are integrated at the same package substrate (fig. 1a). It is noted that Eifrig et al does not particularly disclose that a first element and a second element are different processors as specified in claims 13, 44 and 53. Pian et al teaches, in figure 1, elements 10 and 12, that a preprocessor and an encoder can be constructed as two separate processors. And, therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Eifrig et al by constructing a preprocessor and an transcoder as two separate processors as taught by Pian et al as a matter of various variance, and further more, the combination would

result in a system that the first processor and the second processor are integrated at a same package substrate as specified in claim 54.

Regarding to claim 36: Even though, Eifrig et al does not particularly disclose that the buffer memories as used to hold video data payloads and associated video information are the same type of buffer memory nor they are of the different type of memory; however, in the absence of any contradictory teachings, it would have been obvious to one of ordinary skilled in the art at the time the invention was made to construct the first memory and the second memory as of the same type of memory for the sake of simplicity.

Regarding to claims 55-57: It would have been obvious to one of ordinary skill in the art at the time the invention was made to keep a format of the plurality of packets independent from a video standard of the video data, since it would help to save time by not having to modify the system to comply with ever changing digital video standard.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhon T. Diep whose telephone number is 571-272-7328. The examiner can normally be reached on m-f.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mehrdad Dastouri can be reached on 571-272-7418. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ND

/Nhon T Diep/
Primary Examiner, Art Unit 2621